APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,020	03/08/2001	Ashley Saulsbury	016747015210	4703

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EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	7

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _3/8/01;4/4/01;9/24/01;10/15/01;2/12/02_ .

2a)☐ This action is **FINAL**.　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-20_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-20_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

　　If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____ .

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

　　a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _5_ .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: .

DETAILED ACTION

Specification

1.   The disclosure is objected to because of the following informalities:

The information cites in cross-references to related applications section in the

present application needs to be updated.

Appropriate correction is required.

2.   Claim 19 is objected to because of the following informalities:

Claim 19 should be canceled because it has the same limitations as cited in claim

18.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
subject matter which the applicant regards as his invention.

4.   Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the

invention.

Re claim 2, the limitation "n sub-instructions" lacks an antecedence basis. For

examination purposes, the examiner considers this limitation as the sub-instructions of

loading and storing the sub-subset of matrix elements into appropriate locations that is

different from the first instruction.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sidwell et al.

(U.S. 5,875,355).

Re claim 1, Sidwell et al. disclose in Figures 7, 10, and 15 a method for

processing a matrix of elements in a processor (abstract discloses the processes of

transposing the matrix), the method comprising steps of: loading a first subset of matrix

elements from a first location (Figure 10 reading from SRC1 to 170); loading a second

subset of matrix elements from a second location (Figure 10 reading from SRC2 to 172);

storing a third subset of matrix elements in a first destination (Figure 10 storing into 176);

and storing a fourth subset of matrix elements in a second destination (Figure 10 storing

into 174), wherein the loading and storing steps result from a first instruction issue (160

OPCODE and Zip Instruction of 192).

Re claim 2, Sidwell et al. further disclose in Figure 10 sub-instructions perform an

n-by-n matrix transpose (e.g. 180, 182, 184, 186, 190, and both sides which yield to 14

operations/instructions for 14 elements).

Re claim 3, Sidewell et al. further disclose in Figure 10 the first loading step is performed with a first processing path (path SRC1 to 170) and the second loading step is performed with a second processing path (path SRC2 to 170).

Re claim 4, Sidewell et al. further disclose in Figures 10 and 15 comprising steps of: loading a first subset of matrix elements from a fifth location; loading a sixth subset of matrix elements from a sixth location; storing a seventh subset of matrix elements in a third destination; and storing eighth subset of matrix elements in a fourth destination (these instruction is further processes another subset of matrix e.g. 3rd and 4th rows).

Re claim 5, Sidewell et al. further disclose in Figure 15 the loading and storing steps introduced result from a second instruction issue (Zip interleaved rows of 32 bit objects or flips instruction).

Re claim 6, Sidewell et al. further disclose in Figure 15 each of the first through fourth destination includes a matrix column (any elements in the table).

Re claim 7, Sidewell et al. further disclose in Figure 15 each the first through fourth locations include a matrix row (any elements in the table).

Re claim 8, Sidewell et al. further disclose in Figures 7 and 15 the third and fourth subsets each comprise elements from the first and second subsets (3rd table of Figure 15).

Re claim 9, it is a processing claim of claim 3. Thus, claim 9 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 10, Sidewell et al. further disclose in Figure 10 the 1st through 4th registers each include a plurality of source fields, and each source field includes a matrix element (S1[X] and S2[X]).

Re claim 11, Sidewell et al. further disclose in Figure 10 the 1st and 2nd

destination registers each include a plurality of result fields and each source field includes

a matrix element (174 and 176).

Re claim 12, Sidewell et al. further disclose in Figure 10 wherein 1st and 2nd

instruction processors; and an exchange path between the first and second instruction

processors (180, 182, 184, 186, 188, and 190).

Re claim 13, Sidewell et al. further disclose in Figure 10 the 1st processing path

receives a 1st sub-instruction and the 2nd processing path receives a 2nd sub-instruction

(output from 192 that goes into 180, 182, 184, 186, 188, and 190).

Re claim 14, it is a processing claim of claim 7. Thus, claim 14 is also rejected

under the same rationale in the rejection of rejected claim 7.

Re claim 15, it is a processing claim of claim 6. Thus, claim 15 is also rejected

under the same rationale in the rejection of rejected claim 6.

Re claim 16, Sidewell et al. further disclose in Figures 7-8, 10, and 15 the 1st and

2nd destination registers are addressed by a 1st and 2nd sub-instructions which are included

in a VLIW (Zip, Unzip, Flip instruction).

Re claim 17, it is a method claim of claim 3. Thus, claim 17 is also rejected under

the same rationale in the rejection of rejected claim 3.

Re claims 18-19, Sidewell et al. further disclose in Figures 10 and 12 the 1st and

2nd instructions include a first operation code and the third and fourth instructions include

a second operation code different from the first operation code (160 in Figure 10 and 160

in Figure 12).

Re claim 20, it is a method claim of claim 16. Thus, claim 20 is also rejected

under the same rationale in the rejection of rejected claim 16.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

a.   U.S. Patent No. 5,644,517 to Ho discloses a method for performing matrix

transposition on a mesh multiprocessor architecture having multiple processor with

concurrent execution of the multiple processors.

b.   U.S. Patent No. 5,757,432 to Dulong et al. disclose a manipulating video and

audio signals using a processor which supports SIMD instructions.

c.   U.S. Patent No. 6,115,812 to Abdallah et al. disclose a method and apparatus for

efficient vertical SIMD computations.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The

examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the

organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.
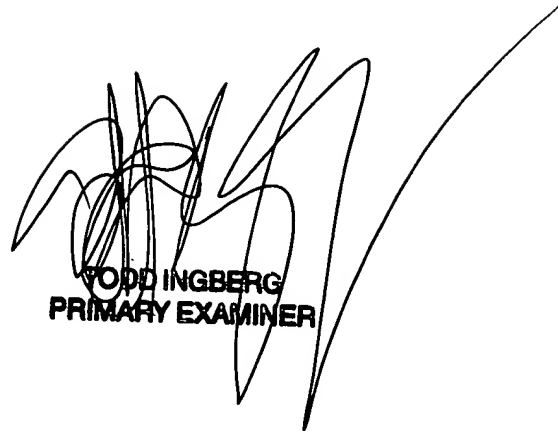
                                                Chat C. Do

Examiner
Art Unit 2124

October 28, 2003

TODD INGBERG
PRIMARY EXAMINER